MachXO3D Breakout Board

User Guide

FPGA-UG-02084-0.90

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DIP	Dual in-line Package
ESB	Embedded Security Block
FPGA	Field Programmable Gate Array
FTDI	Future Technology Devices International
I^2C	Inter-Integrated Circuit
LED	Light Emitting Diode
LUT	Look Up Table
PCB	Printed Circuit Board
RoHS	Restriction of Hazardous Substances Directive
SPI	Serial Peripheral Interface
USB	Universal Serial Bus
WDT	Watchdog Timer
DNI	Do Not Install

1. Introduction

This user guide describes how to start using the MachXO3D™ Breakout Board, hereinafter referred to as the Board. It is an easy-to-use platform for evaluating and designing with the MachXO3D device, a secure control PLD from Lattice Semiconductor. Along with the Board and accessories, a preloaded demonstration design is included. You may also reprogram the onboard MachXO3D device to review your own custom designs.

The MachXO3D Breakout Board currently features a Flash-based MachXO3D-9400HC device in a 256-ball 0.8 mm pitch caBGA package. The Board includes a serial Flash memory for demonstrating external SPI boot-up. The external Flash memory also supports one of the dual-boot modes in addition to on chip dual-boot configuration memory. For more details regarding the supported dual-boot mode, refer to MachXO3D Programming and Configuration Usage Guide (FPGA-TN-02069).

See also the Ordering Information section for more information.

Note: Static electricity can severely shorten the lifespan of electronic components. See the Storage and Handling section of this document for handling and storage tips.

2. Features

The MachXO3D Breakout Kit includes:

- **MachXO3D Breakout Board** – The Board is a 3” × 3” form factor that features the following onboard components and circuits:
  - MachXO3D FPGA – Flash-based LCMXO3D-9400HC-5BG256C
  - USB mini-B connector for power and programming
  - 16 Mb Serial Flash Memory (Machronix MX25V1635) for external SPI boot up support
  - Eight LEDs
  - Four-position DIP switch
  - Momentary push button switch
  - 40-hole prototype area
  - Four 2 × 20 expansion header landings for general I/O, JTAG, and external power
  - 1 × 8 expansion header landing for JTAG
  - 1 × 6 expansion header landing for SPI/I2C
  - 3.3 V and 1.2 V supply rails
- **Preloaded Demo** – The Board includes a preloaded counter design that highlights use of the embedded MachXO3D oscillator and programmable I/O configured for LED drive.
- **USB Connector Cable** – The Board is powered from the USB mini-B socket when connected to a host PC. The USB channel also provides a programming interface to the MachXO3D JTAG port.
- **Lattice Development Kits and Boards Web Page** – Visit www.latticesemi.com/boards, and look for the MachXO3D Breakout Board for the latest documentation including this guide and other downloads supporting this board. This user guide includes demo operation, programming instructions, top-level functional descriptions of the MachXO3D Breakout Board, descriptions of the on-board connectors, and a complete set of schematics.

Figure 2.1 and Figure 2.2 show the top side and bottom side of the MachXO3D Breakout board.

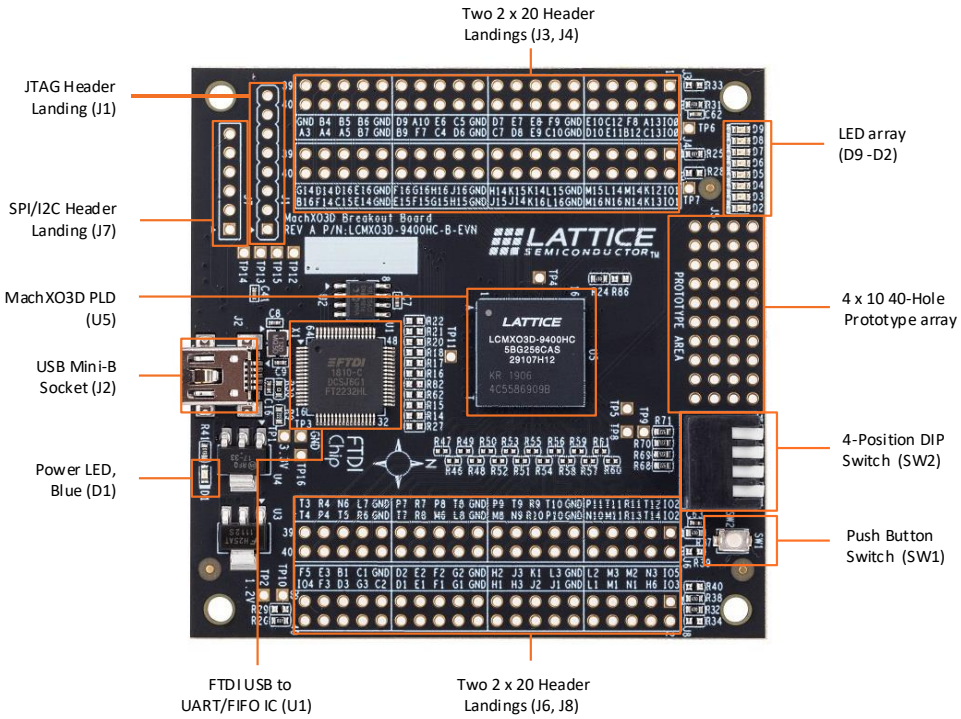


Figure 2.1. MachXO3D Breakout Board, Top Side

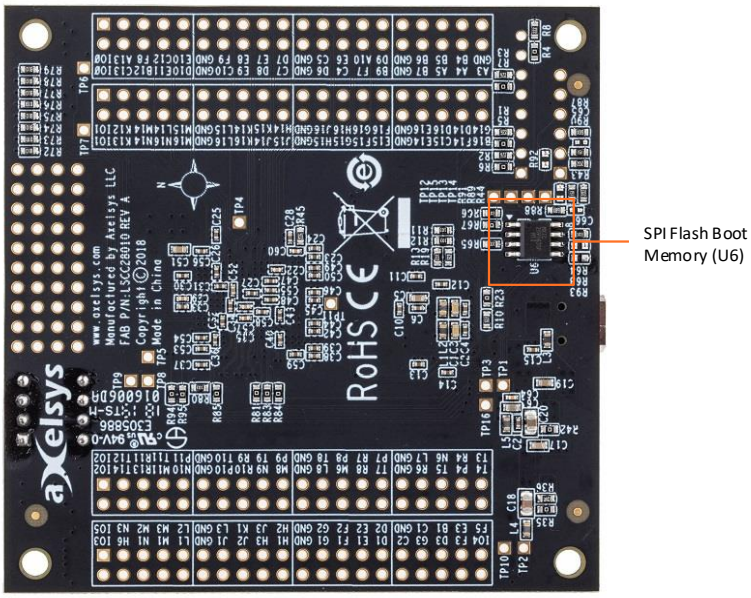


Figure 2.2. MachXO3D Breakout Board, Bottom Side

3. Storage and Handling

Static electricity can shorten the lifespan of electronic components. Follow the tips below to prevent damage that could occur from electrostatic discharge:

- Use anti-static precautions such as operating on an anti-static mat and wearing an anti-static wristband.
- Store the evaluation board in the packaging provided.
- Touch a metal USB housing to equalize voltage potential between you and the Board.

4. Software Requirements

Before you begin developing new designs for the MachXO3D Breakout Board, install the Lattice Diamond® design software. For detailed information on the Diamond software, visit www.latticesemi.com/diamond.

Diamond software includes the Lattice Diamond Programmer for programming your own content to the MachXO3D FPGA. Lattice Diamond Programmer is also available as a stand-alone installation at www.latticesemi.com/programmer

Note: To communicate with the Board, FTDI Chip USB hardware drivers are required. It can be installed as an option within the Diamond or Diamond Programmer installation.

5. MachXO3D Device

The Board currently features the MachXO3D-9400HC FPGA which enhances Secure Control PLD functionality with Hardware Root-of-Trust and Dual Boot capabilities. It features an immutable Embedded Security Block which offers cryptographic functions such as ECDSA256, SHA256, HMAC, ECIES, ECDH, AES-128/256, PUF, Public/Private Key Generation, and True Random Number Generator. Along with Embedded Security Block (ESB), numerous system functions are included, such as two PLLs, 432 kbits of embedded RAM, plus hardened implementations of I^2C and SPI. Flexible, high performance I/O supports numerous single-ended and differential standards including LVDS. The 256-ball BGA package provides up to 206 user I/O in a 14 mm × 14 mm form factor. A complete description of this MachXO3D device can be found in the MachXO3D Device Family Data Sheet (FPGA-DS-02026).

6. Demonstration Design

Lattice provides a simple, pre-programmed demo to illustrate basic operation of the MachXO3D device. The design integrates an LED controller with the on-chip oscillator or external clock. The pre-programmed design resides in the internal Flash.

Note: To restore the factory default demo and program it with other Lattice-supplied examples, see the Download Demo Designs section of this document.

6.1. Running the Demonstration Design

Figure 6.1 is the block diagram of the demonstration design. Upon power-up, the preprogrammed demonstration design automatically loads and drives the LED array in a 1-Hz pattern. The program shows a clock divider driven by either the MachXO3D internal oscillator or the external FTDI clock chip. The divider modules, heartbeat.v and kitcar.v, are clocked at the default frequency of 12 MHz, which divides the clock to cycle the LED display approximately once per second. The resulting light pattern is determined by the DIP Switch (SW2) setting as shown in Table 6.1.

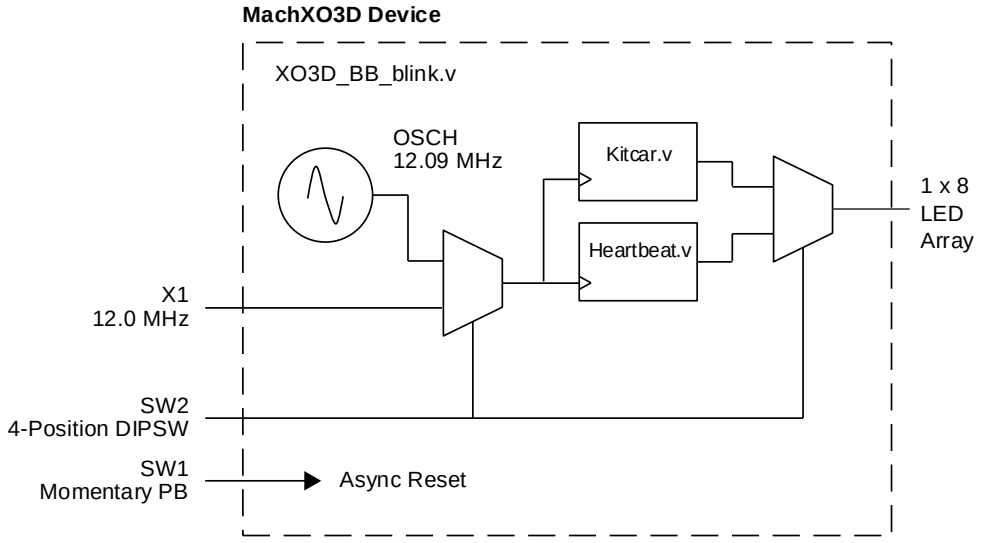


Figure 6.1.Demonstration Design Block Diagram

Table 6.1. DIP Switch Setting and LED Behavior

Switch	Setting	LED Behavior
DIP_SW[1]	0 (Down)	External 12.0 MHz (X1)
	1 (Up)	Internal 12.09 MHz (OSCJ)
DIP_SW[2:4]	001	1 Hz Sweep
	011	1 Hz Left-Right
	111	1 Hz Blink
	Others	1 Hz Alternating

***WARNING**: Do not connect the Board to your PC before you complete the driver installation procedure of this section.*

Communication between the Board and a PC through the USB connection cable requires installation of the FTDI Chip USB hardware drivers. Loading these drivers enables the computer to recognize and program the Board. Drivers can be loaded as part of the installation of Lattice Diamond design software or Diamond Programmer, or as a stand-alone package.

To load the FTDI Chip USB hardware drivers as part of the Lattice Diamond installation:

1. Select **Programmer Drivers** in the **Product Options** of Lattice Diamond Setup.
2. Select **FTDI Windows USB Driver** or **All Drivers** in the **LSC Drivers Install/Uninstall** dialog box.
3. Click **Finish** to install the USB driver.
4. After the driver installation is completed, connect the USB cable from a USB port on your PC to the Board USB mini-B socket (J2). After the connection is made, a blue Power LED (D1) lights indicating the Board is powered on.
5. The demonstration design automatically loads and drive the LED array in a repeating pattern.

To load the FTDI Chip USB hardware drivers through the stand-alone package on a Windows system:

1. Download the FTDI Chip USB hardware driver package from Lattice web site.
2. Extract the FTDI Chip USB hardware driver package to your PC hard drive.
3. Connect the USB cable from a USB port on your PC to the Board USB mini-B socket (J2). After the connection is made, a blue Power LED (D1) lights indicating the Board is powered on.
4. If you are prompted *Windows may connect to Windows Update* select **No, not this time** from available options and click **Next** to proceed with the installation.
5. Choose the **Install from specific location (Advanced)** option and click **Next**.
6. Search for the best driver in these locations and click the **Browse** button to browse to the Windows driver folder. Select the **CDM 2.04.06 WHQL Certified folder** and click **OK**.
7. Click **Next**. A screen displays as Windows copies the required driver files. Windows displays a message indicating that the installation is successful.
8. Click **Finish** to install the USB driver.
9. The demonstration design is automatically loaded and drives the LED array in a repeating pattern.

See the Troubleshooting section of this guide if the Board does not function as expected.

6.2. Download Demo Designs

The LED controller demo is pre-programmed into the Board, however, over time it is likely your board is modified. Lattice distributes source and programming files for demonstration designs compatible with the MachXO3D Breakout Board. The demo design for the Board is available on Lattice website.

To download demo designs:

1. Go to www.latticesemi.com/boards. Navigate to the MachXO3D Breakout Board web page. In the **Documentation** section, from the **Downloads** area, click **Design File**. From the drop-down list, select **MachXO3D Breakout Board Program** and save the file.
2. Extract the contents of MachXO3D_Breakout_Brd.zip to an accessible location on your hard drive.
3. Open the project file Blink.ldf in the Lattice Diamond design software.
4. Run the Process Flow and regenerate the Bitstream file.

After downloading demo designs, you can follow steps in the Programming a Demo Design with the Lattice Diamond Programmer section to program a demo design.

6.3. Programming a Demo Design with the Lattice Diamond Programmer

The demonstration design is pre-programmed into the MachXO3D Breakout Board by Lattice Semiconductor. If you have changed the design but now want to restore the Board to factory settings, follow the steps below.

To program the MachXO3D device:

1. Install, license, and run Lattice Diamond software. See Lattice Diamond for downloading and licensing information.
2. Connect the USB cable to the host PC and the MachXO3D Breakout Board.
3. From Diamond, open the project file Blink.ldf.
4. Double click impl.xcf under Programming Files of imple1 to open the embedded Programmer.
5. Click the **Program** icon. When the process is completed, PASS is displayed in the Status column.

You can also use the stand-alone Diamond Programmer to update the MachXO3D device.

1. Click the **Programmer** icon.
2. Click **Detect Cable**. The Programmer detects the cable HW-USBN-2B, Port: FTUSB-0. If the cable is not detected, see the Troubleshooting section.
3. Click **Device Properties**.
4. Make sure the default Access mode is **Flash Programming Mode**, the default Port Interface is **JTAG Interface**, and the default Operation is **Flash Erase, Program, Verify**.
5. Check the **Flash_A Programming Options**, and select Blink_impl1_a.jed programming file before clicking **OK**.
6. Click the **Program** icon. When the process is completed, PASS is displayed in the Status column.

7. MachXO3D Breakout Board

This section describes the features of the MachXO3D Breakout Board in detail.

7.1. Overview

The MachXO3D Breakout Board is a complete development platform for the MachXO3D FPGA. The Board includes a prototyping area, a USB program/power port, an LED array, switches, and header landings with electrical connections to most of the FPGA programmable I/O, power, and configuration pins. The Board is powered by the PC USB port or optionally with external power. You may create or modify the program files and reprogram the Board using Lattice Diamond software.

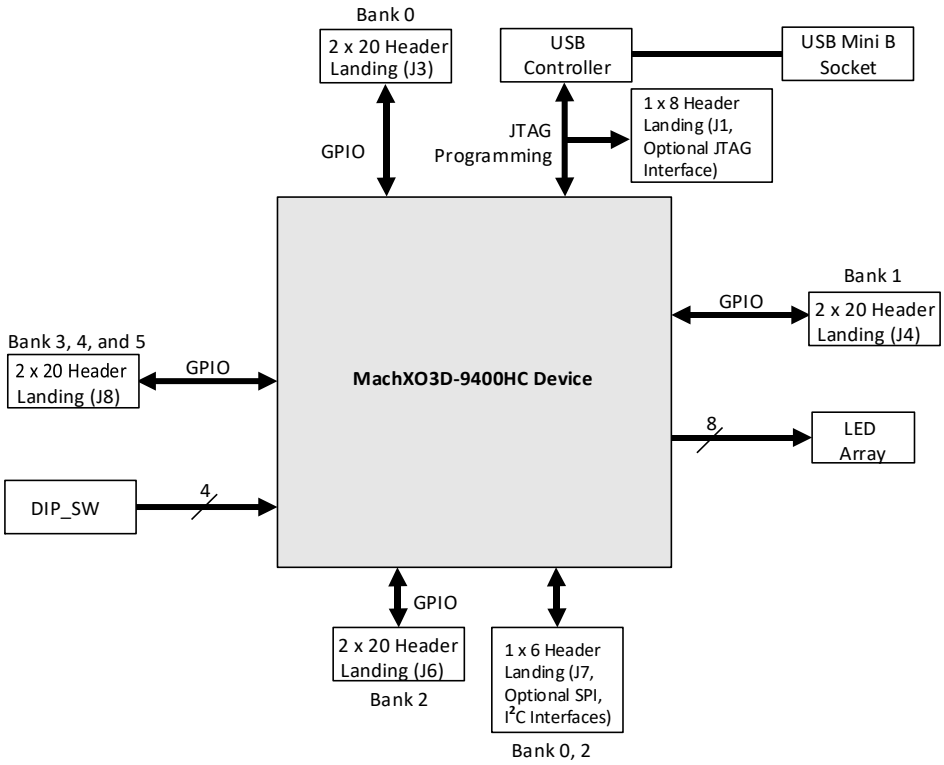


Figure 7.1. MachXO3D-9400HC Block Diagram

Table 7.1. MachXO3D Breakout Board Components and Interfaces

Component/Interface	Type	Schematic Reference	Description
Circuits			
USB Controller	Circuit	U1: FT2232H	USB-to-JTAG interface and dual USB UART/FIFO IC
USB Mini-B Socket	I/O	J2:USB_MINI_B	Programming and debug interface
Components			
LCMXO3D	FPGA	U5: LCMXO3D-9400HC-5BG256C	9400-LUT device packaged in a 14 mm × 14 mm, 256-ball caBGA
Interfaces			
LED Array	Output	D9-D2	Red LEDs
Push Button Switch	Input	SW1	Momentary User Input
4-position DIP Switch	Input	SW2	User inputs
Four 2 x 20 Header Landings	I/O	J3: header_2x20 J4: header_2x20 J6: header_2x20 J8: header_2x20	User-definable I/O
1 x 8 Header Landing	I/O	J1: header_1x8	Optional JTAG interface
1 x 6 Header Landing	I/O	J7: header_1x6	Optional SPI/I^2C interfaces
4 x 10 40-Hole Prototype Area	—	—	Prototype area 100 mil centered holes.
Test Points	Power	TP1: +3.3 V TP2: +1.2 V TP3: GND	Power and ground reference points

7.2. Subsystems

This section describes the principle subsystems for the MachXO3D Breakout Board in alphabetical order.

7.2.1. Clock Sources

Clock sources for the LED demonstration designs originate from the MachXO3D on-chip oscillator or the 12 MHz crystal X1. You may use an expansion header landing to drive an FPGA input with an external clock source.

7.2.2. Expansion Header Landings

The expansion header landings provide access to user GPIOs, primary inputs, clocks, and VCCO pins of the MachXO3D device. The remaining pins serve as power supplies for external connections. Each landing is configured as one 2 × 20 100 mil.

Table 7.2. Expansion Connector Reference

Item	Description
Reference Designators	J3, J4, J6, J8
Part Number	header_2x20

Table 7.3. Expansion Header Pin Information for Bank 0 (J3)

Header Pin Number	–9400HC Function	MachXO3D Ball in 256caBGA
1	VCCIO0	D5,D12,G8,G9
2	VCCIO0	D5,D12,G8,G9
3	PT44C/INITn	A13
4	PT44D/DONE	C13
5	PT27A	F8
6	PT43B	B12
7	PT43A	C12
8	PT29B	E11
9	PT31B	E10
10	PT31A	D10
11	GND	—
12	GND	—
13	PT29A	F9
14	PT31C/JTAGENB	C10
15	PT22B	E8
16	PT24B	E9
17	PT15B	E7
18	PT24A	D8
19	PT21B	D7
20	PT20B	C7
21	GND	—
22	GND	—
23	PT10B	C5
24	PT15A	D6
25	PT21A	E6
26	PT9A	C4
27	PT28B	A10
28	PT22A	F7
29	PT27B	D9
30	PT28A	B9
31	GND	—
32	GND	—
33	PT11B	B6
34	PT20A	B7
35	PT9B	B5
36	PT11A	A5
37	PT12B	B4
38	PT10A	A4
39	GND	—
40	PT12A	A3

Table 7.4. Expansion Header Pin Information for Bank 1 (J4)

Header Pin Number	–9400HC Function	MachXO3D Ball in 256caBGA
1	VCCIO1	E13,H10,J10,M13
2	VCCIO1	E13,H10,J10,M13
3	PR24D	K12
4	PR24C	K13
5	PR28A	M14
6	PR29B	N14
7	PR21B	L14
8	PR29A	N16
9	PR28B	M15
10	PR25B	M16
11	GND	—
12	GND	—
13	PR25A	L15
14	PR21A	L16
15	PR20A	K14
16	PR19B	K16
17	PR20B	K15
18	PR18B	J14
19	PR17A/PCLKT1_0	H14
20	PR19A	J15
21	GND	—
22	GND	—
23	PR18A	J16
24	PR16B	H15
25	PR17B/PCLKC1_0	H16
26	PR12A	G15
27	PR16A	G16
28	PR5B	F15
29	PR7B	F16
30	PR2B/R_GPLLC_FB	E15
31	GND	—
32	GND	—
33	PR5A	E16
34	PR3B/R_GPLLC_IN	E14
35	PR3A/R_GPLLT_IN	D16
36	PR2C	C15
37	PR2A/R_GPLLT_FB	D14
38	PR7A	F14
39	PR12B	G14
40	PR2D	B16

Table 7.5. Expansion Header Pin Information for Bank 2 (J6)

Header Pin Number	–9400HC Function	MachXO3D Ball in 256caBGA
1	VCCIO2	K8,K9,N5,N12
2	VCCIO2	K8,K9,N5,N12
3	PB43B	T12
4	PB41B	T14
5	PB43A	R11
6	PB41A	R13
7	PB35A	T11
8	PB32B	M11
9	PB35B	P11
10	PB32A	N10
11	GND	—
12	GND	—
13	PB30B	T10
14	PB33A	P10
15	PB30A	R9
16	PB33B	R10
17	PB29A/PCLKT2_1	T9
18	PB27B	N9
19	PB29B/PCLKC2_1	P9
20	PB27A	M8
21	GND	—
22	GND	—
23	PB24B	T8
24	PB21B	L8
25	PB24A	P8
26	PB21A	M6
27	PB18A	R7
28	PB22B/PCLKC2_0	R8
29	PB18B	P7
30	PB22A/PCLKT2_0	T7
31	GND	—
32	GND	—
33	PB13B	L7
34	PB10B	R6
35	PB13A	N6
36	PB10A	T5
37	PB8B	R4
38	PB5A	P4
39	PB8A	T3
40	PB5B	T4

Table 7.6. Expansion Header Pin Information for Bank 3/4/5 (J8)

Header Pin Number	–9400HC Function	MachXO3D Ball in 256caBGA
1	VCCIO5	E4
2	VCCIO3	M4
3	PL30B	N3 (Bank 3)
4	PL12D	H6 (Bank 5)
5	PL30A	M2 (Bank 3)
6	PL29B	N1 (Bank 3)
7	PL29A	M3 (Bank 3)
8	PL27B/PCLKC3_0	M1 (Bank 3)
9	PL27A/PCLKT3_0	L2 (Bank 3)
10	PL25A	L1 (Bank 3)
11	GND	—
12	GND	—
13	PL25B	L3 (Bank 3)
14	PL16A/PCLKT4_0	J1 (Bank 4)
15	PL17B	K1 (Bank 4)
16	PL17A	J2 (Bank 4)
17	PL16B/PCLKC4_0	J3 (Bank 4)
18	PL14A	H3 (Bank 4)
19	PL13B	H2 (Bank 4)
20	PL14B	H1 (Bank 4)
21	GND	—
22	GND	—
23	PL12A	G2 (Bank 5)
24	PL13A	G1 (Bank 4)
25	PL7B/PCLKC5_0	F2 (Bank 5)
26	PL11B	F1 (Bank 5)
27	PL4A/L_GPLLT_IN	E2 (Bank 5)
28	PL7A/PCLKT5_0	E1 (Bank 5)
29	PL4D	D2 (Bank 5)
30	PL3B/L_GPLLC_FB	D1 (Bank 5)
31	GND	—
32	PL2D	C2 (Bank 5)
33	PL4C	C1 (Bank 5)
34	PL12B	G3 (Bank 5)
35	PL2C	B1 (Bank 5)
36	PL3A/L_GPLLT_FB	D3 (Bank 5)
37	PL4B/L_GPLLC_IN	E3 (Bank 5)
38	PL11A	F3 (Bank 5)
39	PL12C	F5 (Bank 5)
40	VCCIO4	H7,J7

J3

1	2
VCCIO0	VCCIO0
A13	C13
F8	B12
C12	E11
E10	D10
GND	GND
F9	C10
E8	E9
E7	D8
D7	C7
GND	GND
C5	D6
E6	C4
A10	F7
D9	B9
GND	GND
B6	B7
B5	A5
B4	A4
GND	A3
39	40

J4

1	2
VCCIO1	VCCIO1
K12	K13
M14	N14
L14	N16
M15	M16
GND	GND
L15	L16
K14	K16
K15	J14
H14	J15
GND	GND
J16	H15
H16	G15
G16	F15
F16	E15
GND	GND
E16	E14
D16	C15
D14	F14
G14	B16
39	40

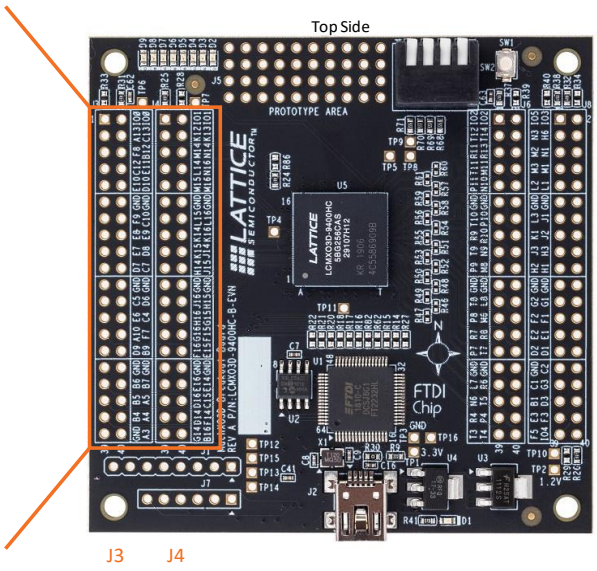
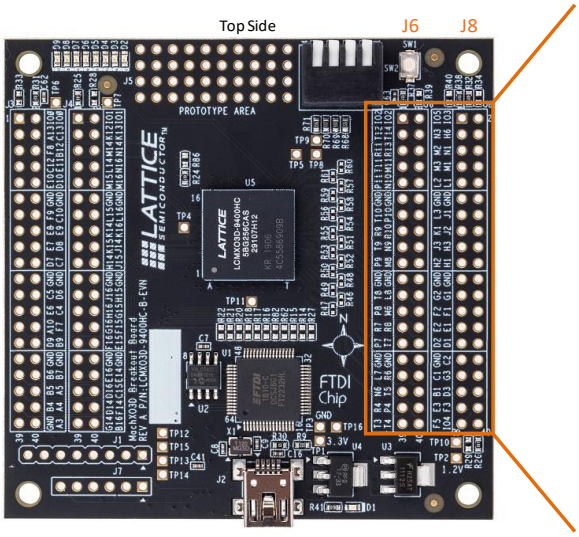


Figure 7.2. J3/J4 Header Landing Callout



J6

1	2
VCCIO2	VCCIO2
T12	T14
R11	R13
T11	M11
P11	N10
GND	GND
T10	P10
R9	R10
T9	N9
P9	M8
GND	GND
T8	L8
P8	M6
R7	R8
P7	T7
GND	GND
L7	R6
N6	T5
R4	P4
T3	T4
39	40

J8

1	2
VCCIO5	VCCIO3
N3	H6
M2	N1
M3	M1
L2	L1
GND	GND
L3	J1
K1	J2
J3	H3
H2	H1
GND	GND
G2	G1
F2	F1
E2	E1
D2	D1
GND	C2
C1	G3
B1	D3
E3	F3
F5	VCCIO4
39	40

Figure 7.3. J6/J8 Header Landing Callout

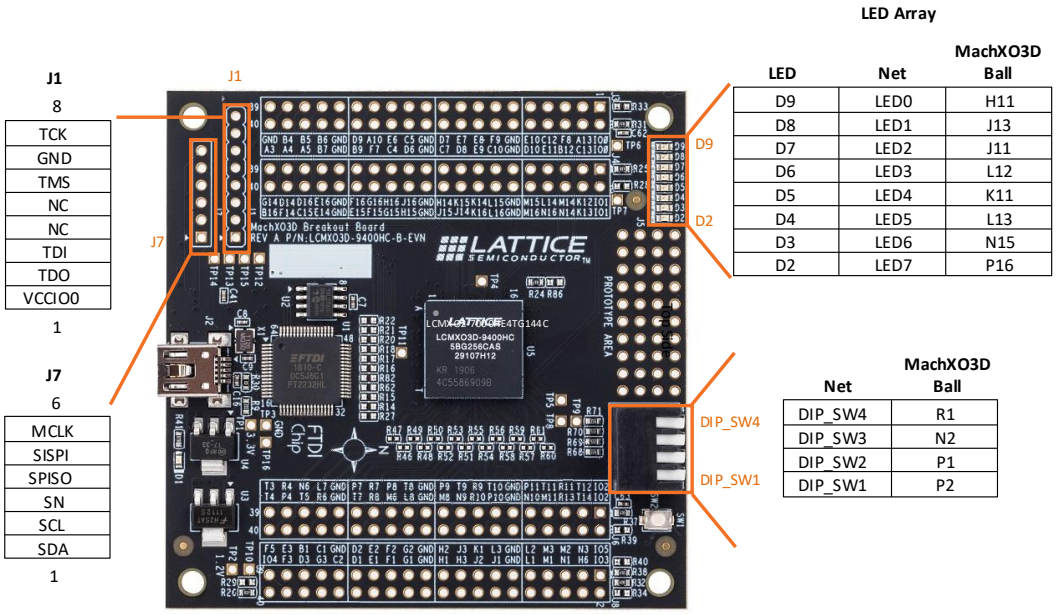


Figure 7.4. J1 Header Landing and LED Array Callout

7.2.3. MachXO3D FPGA

The LCMXO3D-9400HC-5BG256C is a 256-ball caBGA package FPGA device that provides up to 206 usable I/O in a 14 mm × 14 mm package. 150 I/O is accessible from the Board headers, switches, and LEDs.

Table 7.7. MachXO3D FPGA Interface Reference

Item	Description
Reference Designators	U5
Part Number	LCMXO3D-9400HC-5BG256C (Flash)
Manufacturer	Lattice Semiconductor
Web Site	www.latticesemi.com

7.2.4. Programming Interface Circuits

For power and programming an FTDI USB UART/FIFO, IC converter provides a communication interface between a PC host and the JTAG programming chain of the Board. The USB 5 V supply is also used as a source for the 3.3 V supply rail. A USB mini-B socket is provided for the USB connector cable.

Table 7.8. USB/JTAG Interface Reference

Item	Description
Reference Designators	U1
Part Number	FT2232HL
Manufacturer	Future Technology Devices International (FTDI)

Table 7.9. JTAG Programming Pin Information

Description	MachXO3D Ball in 256caBGA
Test Data Output	C6:TDO
Test Data Input	A6:TDI
Test Mode Select	B8:TMS
Test Clock	A7:TCK

Table 7.10. SPI Programming Pin Information

Description	MachXO3D Ball in 256caBGA
Master Clock/Configuration Clock	P6:MCLK/CCLK
Serial Data Input	P13: SI/SISPI
Serial Data Output	T6: SO/SPISO
SPI Slave Select	R12: SN

Table 7.11. I2 Programming Pin Information

Description	MachXO3D Ball in 256caBGA
Serial Data	C9:SDA
Serial Clock	A9:SCL

7.2.5. LEDs

A blue LED (D1) is used to indicate USB 5V power. Eight red LEDs are driven by I/O pins of the MachXO3D device.

Table 7.12. Power and User LEDs Reference

Description	MachXO3D Ball in 256caBGA
Reference Designators	Red LEDs (D2, D3, D4, D5, D6, D7, D8, D9) Blue LEDs (D1)
Part Number	LTST-C190KRKT (D2-D9) LTST-C190TBKT (D1)
Manufacturer	Lite-On It Corporation
Website	www.liteonit.com

7.2.6. Power Supply

3.3 V and 1.2 V power supply rails are converted from the USB 5 V interface when the Board is connected to a host PC.

7.2.7. Test Points

In order to check the various voltage levels used, test points are provided:

- TP1: +3.3 V
- TP2: +1.2 V
- TP3: GND

7.2.8. USB Programming and Debug Interface

The USB mini-B socket of the MachXO3D Breakout Board serves as the programming and debug interface.

JTAG Programming: For JTAG programming, a pre-programmed USB PHY peripheral controller is provided on the MachXO3D Breakout Board to serve as the programming interface to the MachXO3D FPGA.

Programming requires the Lattice Diamond or ispVM System software.

Table 7.13. USB Interface Reference

Item	Description
Reference Designators	U1
Part Number	FT2232HL
Manufacturer	Future Technology Devices International (FTDI)
Website	www.liteonit.com

7.3. Board Modifications

This section describes how to modify to the Board to change or add functionality.

7.3.1. Bypassing the USB Programming Interface

The USB programming interface circuit can be optionally bypassed by removing the 0 Ω resistors: R4, R5, R6, R7 or pulling down FTDI RESET# through TP16. Refer to the USB Programming and Debug Interface section for details about the USB programming interface circuit. See Appendix A. Schematics, Sheet 2 of 8. Header landing J1 provides JTAG signal access for jumper wires or a 1 × 8 pin header.

7.3.2. Applying External Power

The MachXO3D Breakout Board is powered by the circuit of Schematic showed on Sheet 3 of 8 based on the 5 V USB power source. You may disconnect this power source by removing the 0 Ω resistors: R35 (VCC_1.2 V) and R42 (VCC_3.3 V). Power connections are available from the test points, TP1 (+3.3 V) and TP2 (+1.2 V).

7.3.3. Measuring Bank and Core Power

Test points (TP1, TP2) provide access to power supplies of the MachXO3D FPGA. Inline 1 Ω resistors: R31 (VCCIO0, +3.3 V, Bank 0), R25 (VCCIO1, +3.3 V, Bank 1), R37 (VCCIO2, +3.3 V, Bank 2), R32 (VCCIO3, +3.3 V, Bank 3), R26 (VCCIO4, +3.3 V, Bank 4), R38 (VCCIO5, +3.3 V, Bank 5), R24 (VCC core, +3.3 V) can be used to measure current for the power supplies.

7.4. Mechanical Specifications

Dimensions: 3 in. [L] x 3 in. [W] x 1/2 in. [H]

7.5. Environmental Requirements

The Board must be stored between –40° C and 100° C. The recommended operating temperature is between 0° C and 90° C.

The Board can be damaged without proper anti-static handling.

8. Troubleshooting

Use the tips in this section to diagnose problems with the MachXO3D Breakout Board.

8.1. LEDs Do Not Flash

If power is applied but the Board does not flash according to the pre-programmed counter demonstration, then it is likely the Board has been reprogrammed with a new design. Follow the directions in the Demonstration Design section to restore the factory default.

8.2. USB Cable Not Detected

If Lattice Diamond Programmer does not recognize the USB cable after installing the Lattice USB port drivers and rebooting, the incorrect USB driver may have been installed. This usually occurs if you attach the Board to your PC prior to installing the Lattice-supplied USB driver.

To access the Troubleshooting the USB Driver Installation Guide from Lattice Diamond and stand-alone Diamond Programmer:

1. Start Lattice Diamond or Diamond Programmer, and choose **Help**.
2. Search **USB driver** or **Troubleshooting**. Then select the **Troubleshooting the USB Driver** topic.
3. Follow the instructions to install Lattice USB driver.

An alternate failure mode can occur when the user design assigns an output signal to the FPGA package pin C8 that is connected the oscillator (X1) output signal "12 MHz". This can occur unintentionally when the Placer randomly assigns unconstrained outputs. In this case, the contention squelches the FTDI device (U1) clock input, rendering it unable to communicate. To eliminate the contention, remove the resistor R23. This will restore the FTDI device operation and allow the erasure of the offending FPGA image. Resistor R23 should be re-installed if an external clock source is desired.

8.3. Determine the Source of a Pre-programmed Device

If the MachXO3D Breakout Board has been reprogrammed, the original demo design can be restored. To restore the Board to the factory default, see the Download Demo Designs section for details on downloading and reprogramming the device.

9. Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
MachXO3D Breakout Board	LCMXO3D-9400HC-B-EVN	—

Appendix A. Schematics

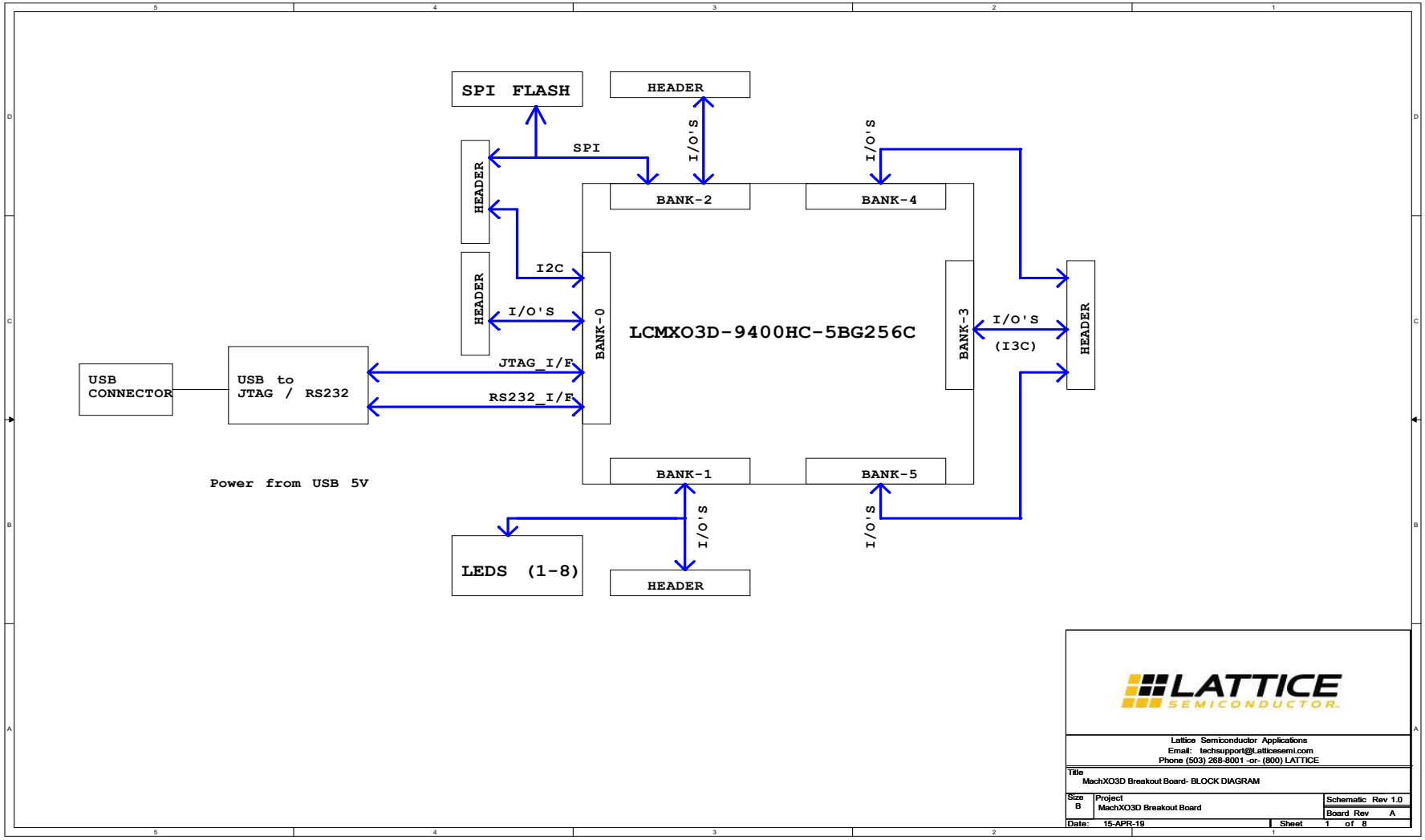


Figure A.1. Block Diagram

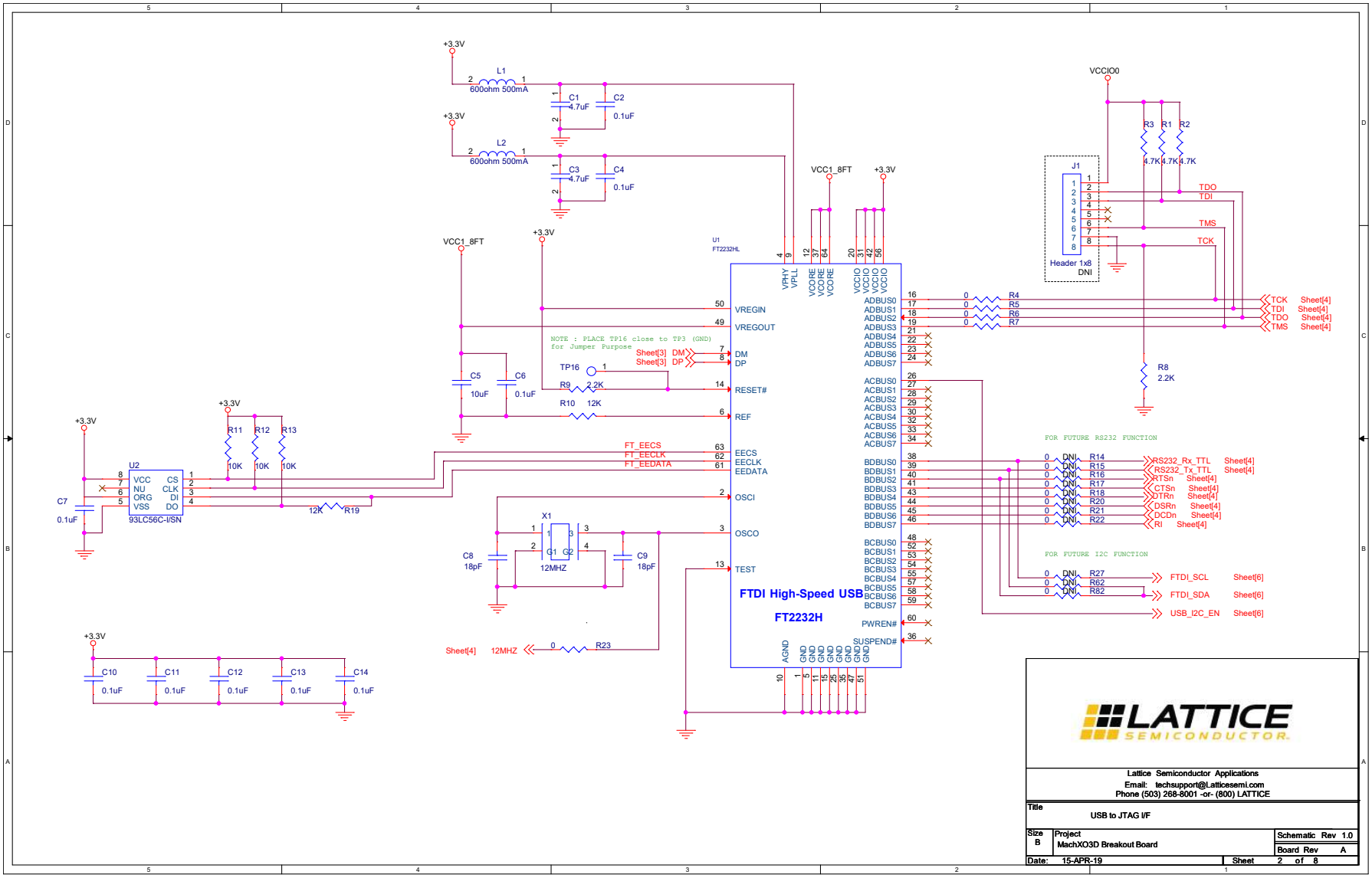


Figure A.2. USB to JTAG Interface

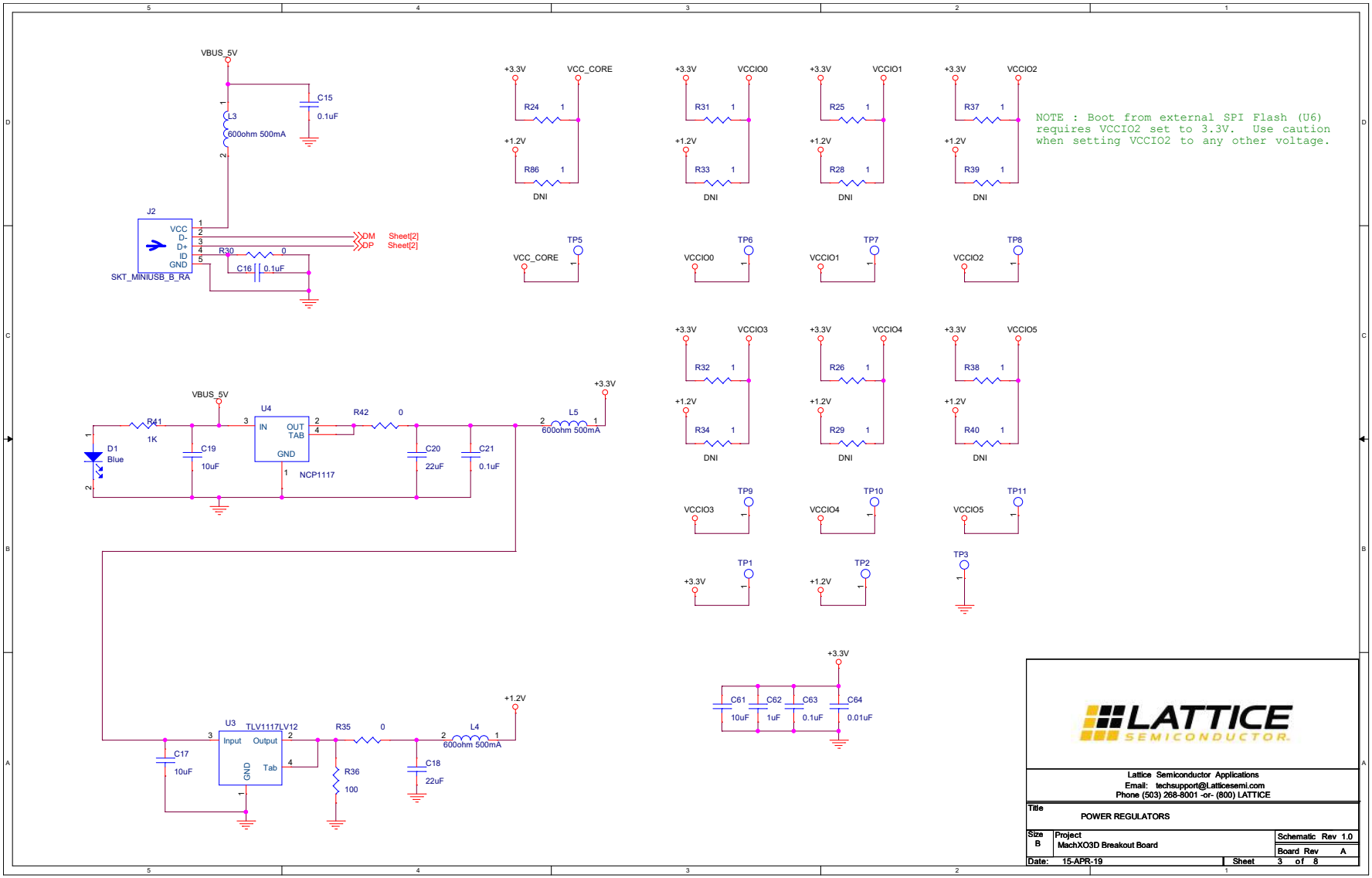


Figure A.3. Power Regulators

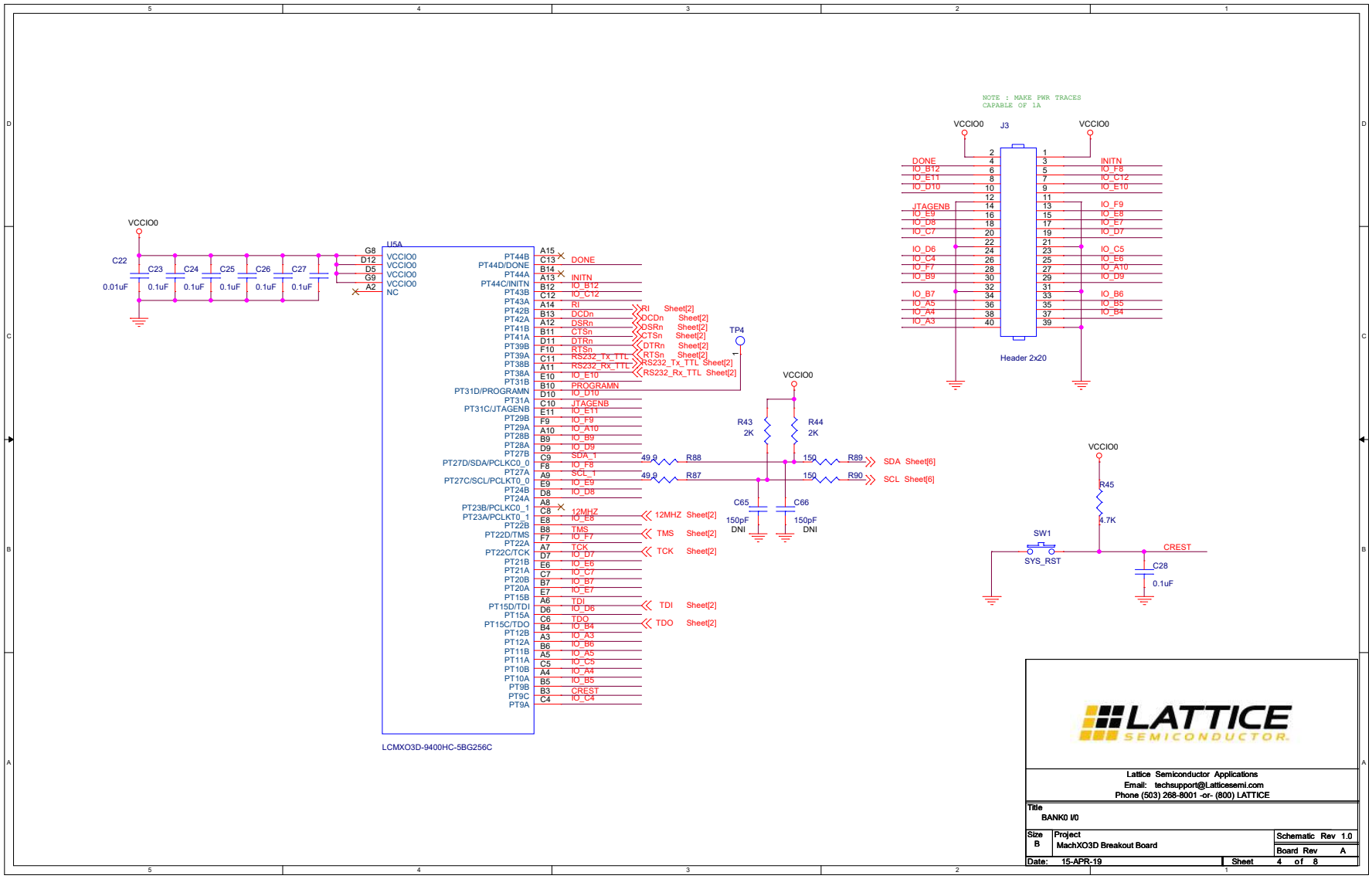


Figure A.4. Bank0 I/O

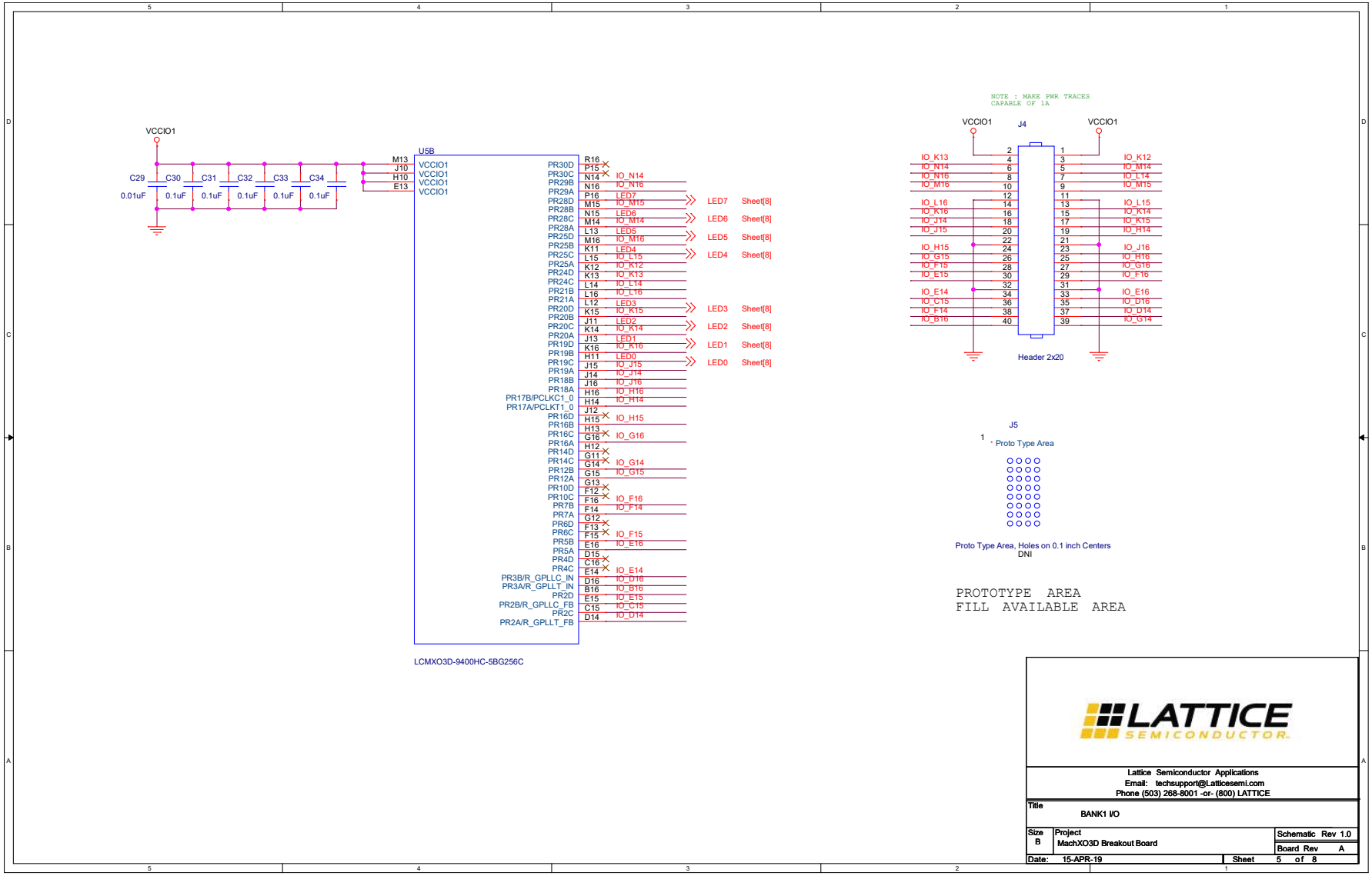


Figure A.5. Bank1 I/O

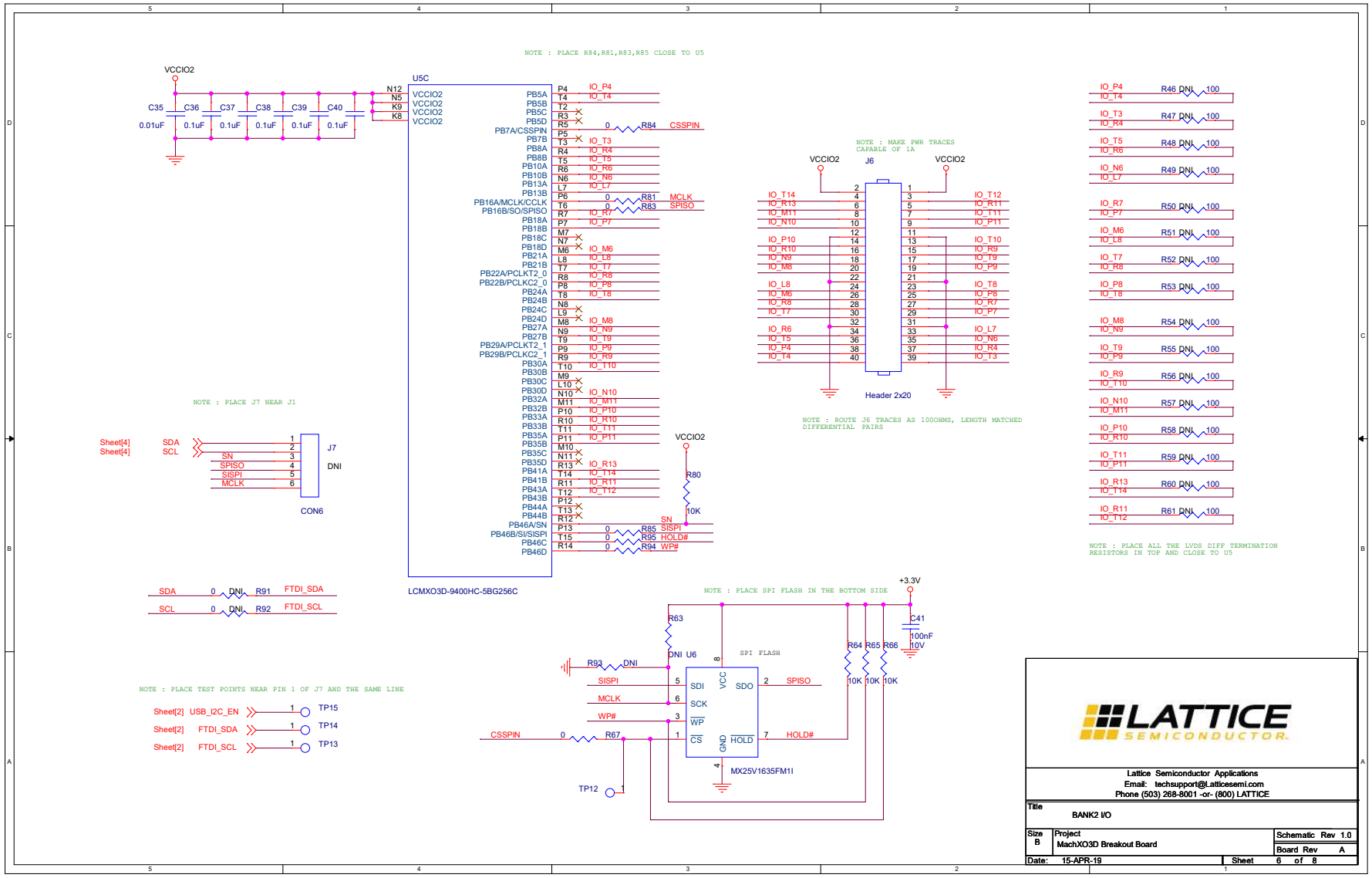


Figure A.6. Bank2 I/O

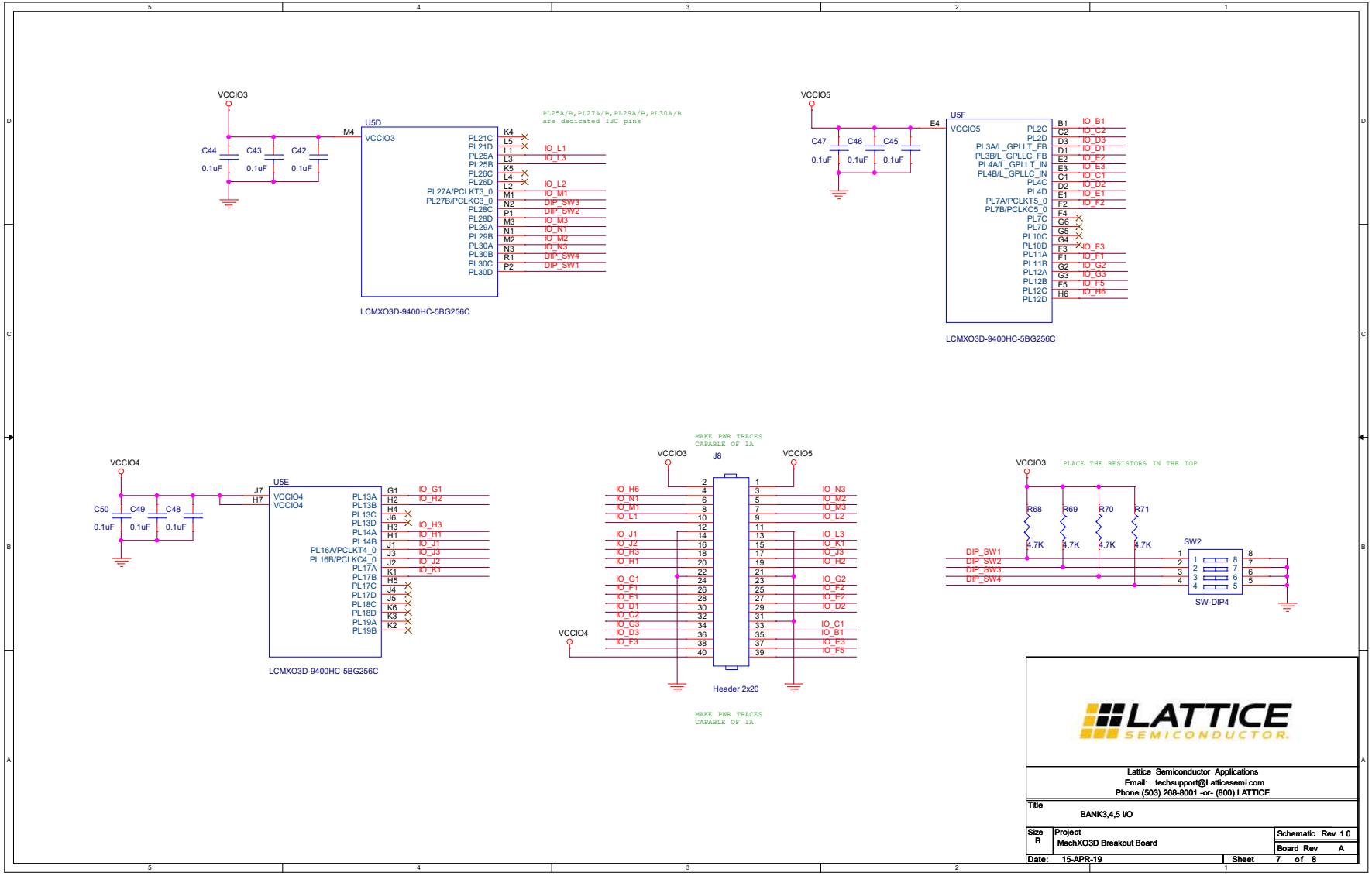


Figure A.7. Bank3, 4, 5 I/O

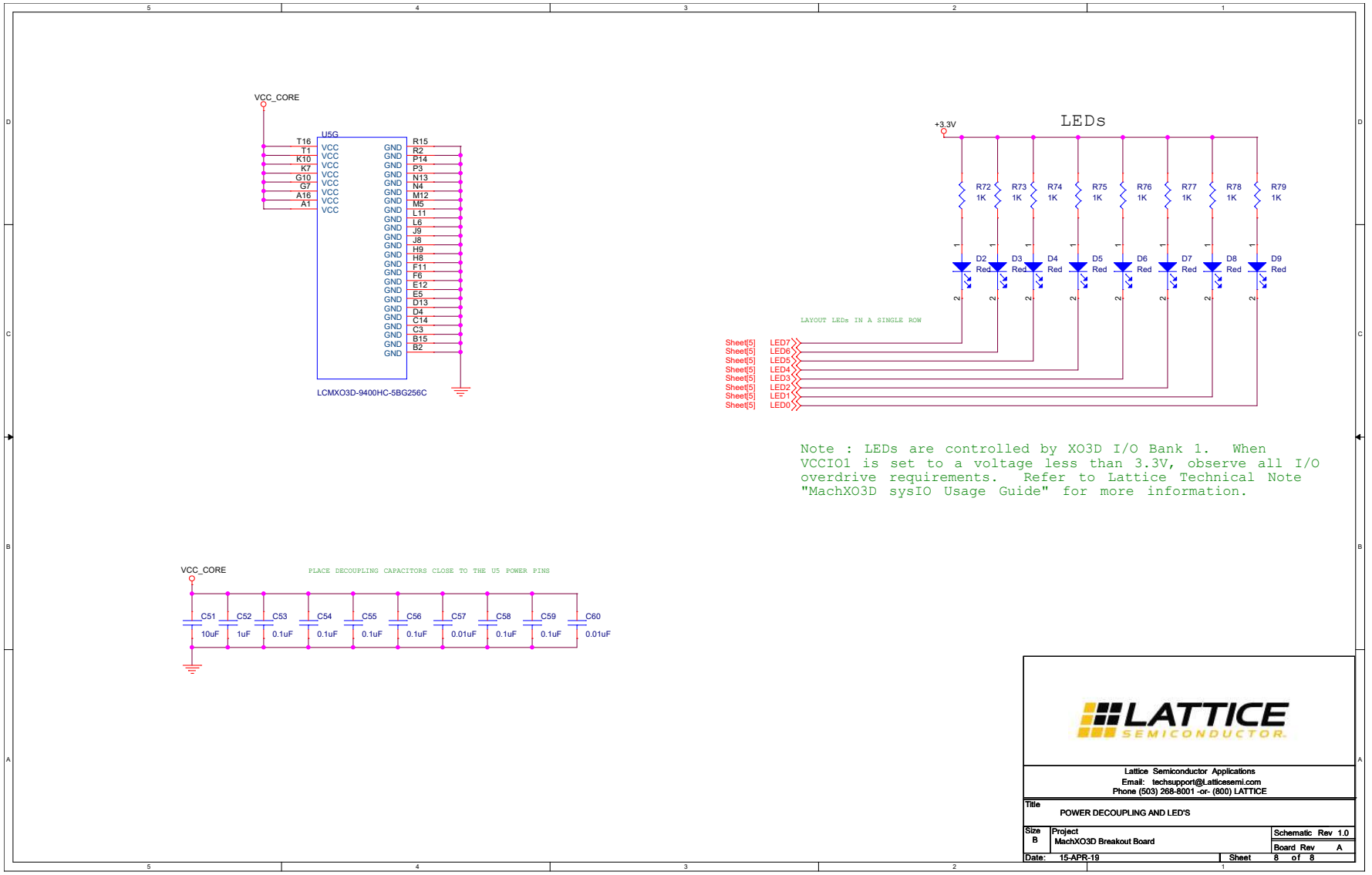


Figure A.8. Power Decoupling and LEDs

Appendix B. Bill of Materials

Table B.1. MachXO3D Breakout Board Bill of Materials

Item	Quantity	Reference	Value	Manufacturer	MFG Pin
1	2	C1,C3	4.7 uF	Panasonic	ECJ-1VB0J475K
2	44	C2,C4,C6,C7,C10,C11,C12,C13,C14, C15,C16,C21,C23,C24,C25,C26,C27, C28,C30,C31,C32,C33,C34,C36,C37, C38,C39,C40,C42,C43,C44,C45,C46, C47,C48,C49,C50,C53,C54,C55,C56, C58,C59,C63	0.1 uF	Kemet	C0402C104K4RACTU
3	5	C5,C17,C19,C51,C61	10 uF	Taiyo Yuden	LMK107BJ106MALTD
4	2	C8,C9	18 pF	Kemet	C0402C180K3GACTU
5	2	C18,C20	22 uF	Taiyo Yuden	LMK212BJ226MG-T
6	6	C22,C29,C35,C57,C60,C64	0.01 uF	Kemet	C0402C103J4RACTU
7	1	C41	100 nF	Murata	GRM155R61A104KA01D
8	2	C52,C62	1 uF	Kemet	C0402C105K9PACTU
9	2	C65,C66	150 pF (DNI)	Kemet	C0402C104K4RACTU
10	1	D1	Blue	LITE-On INC	LTST-C190TBKT
11	8	D2,D3,D4,D5,D6,D7,D8,D9	Red	LITE-On INC	LTST-C190KRKT
12	1	J1	Header 1 x 8	Molex	0022284081
13	1	J2	Mini USB-B	Neltron	5075BMR-05-SM-CR
14	4	J3,J4,J6,J8	Header 2 x 20	Samtec	TSW-120-07-G-D
16	1	J7	Header 1 x 6	Samtec	TSW-106-07-F-S-ND
17	5	L1,L2,L3,L4,L5	600 Ohm 500 mA	Murata	BLM18AG601SN1D
18	8	R1,R2,R3,R45,R68,R69,R70,R71	4.7 K	Vishay	CRCW06034K70FKEA
19	13	R4,R5,R6,R7,R23,R30,R35,R42,R67 ,R81,R83, R84,R85	0	Yageo	RC0603JR-070RL
20	2	R8,R9	2.2 K	Vishay	CRCW06032K20FKEA
21	2	R10,R19	12 K	Yageo	RC0603FR-0712KL
22	7	R11,R12,R13,R64,R65,R66,R80	10 K	Stackpole Electronics Inc	RMCF0603JT10K0
23	15	R14,R15,R16,R17,R18,R20,R21,R2 2,R27,R62, R82,R91,R92,R94,R95	0 (DNI)	Yageo	RC0603JR-070RL
24	7	R24,R25,R26,R31,R32,R37,R38	1	Vishay	CRCW06031R00JNEAHP
25	7	R28,R29,R33,R34,R39,R40,R86	1 (DNI)	Vishay	CRCW06031R00JNEAHP
26	1	R36	100	Yageo	RC0603FR-07100RL
27	9	R41,R72,R73,R74,R75,R76,R7 7,R78,R79	1 K	Yageo	RC0603FR-071KL
28	2	R43,R44	2 K	Vishay	CRCW06032K00JNEA
29	16	R46,R47,R48,R49,R50,R51,R52,R53, R54,R55,R56,R57,R58,R59,R60, R61	100 (DNI)	Yageo	RC0402FR07100RL
30	1	R63, R93	1K (DNI)	Yageo	RC0603FR-071KL
30	2	R87,R88	49.9	Vishay	CRCW060349R9FKEA
31	2	R89,R90	150	Vishay	CRCW0603150RJNEA
32	1	SW1		E-Switch	TL1015AF160QG
33	1	SW2	DIP	CTS Electrocomponents	195-4MST
35	1	U1	—	FTDI	FT2232HL
36	1	U2	—	Microchip	93LC56C-I/SN
37	1	U3	—	TI	TLV1117LV12DCY
38	1	U4	—	On Semi	NCP1117ST33T3G

Item	Quantity	Reference	Value	Manufacturer	MFG Pin
39	1	U5	—	Lattice Semiconductor	LCMXO3D-9400HC-5BG256C LCMXO3LF-6900C-5BG256C
40	1	U6	16Mb	Macronix	MX25V1635FM1I (early builds) or S25FL208K0RMFI041 (later builds)
41	1	X1	12 MHz	TXC	7M-12.000MAAJ-T

References

Lattice Semiconductor Documents

This is a list of the related documents that are available from your Lattice Semiconductor sales representative.

- MachXO3D Family Data Sheet (FPGA-DS-02026)
- MachXO3D Programming and Configuration Usage Guide (FPGA-TN-02069)

Revision History

Revision 0.90, July 2019

Section	Change Summary
All	First preliminary release.

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